CLAIMS

I claim:

1. A memory circuit comprising:

an output data bus;

a memory array receiving a memory address and providing output data from a memory access using the memory address, the memory array comprising a plurality of memory blocks, and a control circuit providing a timing signal that is asserted at a first predetermined time earlier than a second predetermined time when the output data from the memory access is expected to be ready at the output data bus;

a redundant memory circuit receiving the memory address and the timing signal, and providing output data when the memory address corresponds to a stored memory address in the redundant memory circuit, the output data being provided at the first predetermined time, in accordance with the timing signal; and

a selection circuit selecting, for output at the second predetermined time on the data output bus, between the output data of the memory array and the output data of the redundant memory circuit.

2. A memory circuit as in Claim 1, wherein the memory array provides a second timing signal which is asserted to indicate the second predetermined time.

3. A memory circuit as in Claim 2, wherein the selection circuit performs the selecting according to the second timing signal.

4. A memory circuit as in Claim 1, wherein the redundant memory circuit comprises a first-in-first-out

(FIFO) memory that holds the output data of the redundant memory circuit.

5. A memory circuit as in Claim 4, wherein the FIFO memory comprises a control circuit receiving the timing signal.

6. A memory circuit as in Claim 5, wherein the control circuit of the FIFO memory comprises toggle flip-flops.

7. A memory circuit as in Claim 1, wherein the redundant memory circuit comprises a plurality of memory blocks.

8. A memory circuit as in Claim 1, wherein the redundant memory circuit comprises address comparators.

9. A memory circuit as in Claim 1, wherein the memory array comprises a pipelined output stage.

10. In a memory circuit, a method comprising:

receiving into a memory array a memory address for performing an access a memory block within the memory array corresponding to the memory address;

generating, from the memory array, a timing signal that is asserted at a first predetermined time earlier than a second predetermined time when the output data from the memory access is expected to be ready at an output data bus;

receiving into a redundant memory circuit the memory address and the timing signal;

providing from the redundant memory circuit output data when the memory address corresponds to a stored memory address in the redundant memory circuit, the output data

being provided at the first predetermined time in accordance with the timing signal; and

at the second predetermined time, selecting between the output data of the memory array and the output data of the redundant memory circuit for output on the data output bus.

11. A method as in Claim 10, further comprising generating, from the memory array, a second timing signal indicating that the output data of the memory array is ready.

12. A method as in Claim 11, wherein the selecting is performed according to the second timing signal.

13. A method as in Claim 10, wherein the redundant memory circuit holds the output data of the redundant memory circuit in a first-in-first-out (FIFO) memory.

14. A method as in Claim 13, wherein the FIFO memory is controlled according to the timing signal.

15. A method as in Claim 14, wherein the timing signal is provided to control a toggle flip-flop.

16. A method as in Claim 10, wherein the redundant memory circuit comprises a plurality of memory blocks.

17. A method as in Claim 10, further comprising comparing, in the redundant memory circuit, the memory address to the stored memory address using address comparators.

18. A method as in Claim 10, wherein the memory array comprises a pipelined output stage.